WHAT IS CLAIMED IS:

1. A method for chip testing, comprising the steps of:

establishing a communications link between a chip and a computer tester;

receiving on the chip an initial test algorithm over a communications link;

testing the chip, using a built-in self-test circuit (BIST) on the chip, in accordance with the initial test algorithm;

collecting a set of failure information in response to the testing; and

transmitting the failure information from the chip to the computer over the communications link.

2. The method of claim 1, wherein:

the receiving step includes the step of receiving a second test algorithm whose coverage differs from the initial test algorithm; and

the testing step includes the step of testing the chip in accordance with the second test algorithm.

3. The method of claim 1, wherein the testing step includes the step of:

testing a memory array within the chip in accordance with the algorithm.

4. The method of claim 3 further comprising the step of:

generating a bit-map on the computer, from the failure information, of failed bit locations within the memory array.

5. The method of claim 3 wherein the collecting step includes the step of:

collecting a set of failed address information in response to the testing.

6. The method of claim 5 wherein:

the testing step includes the steps of,

writing a set of data to an address under test in the memory array

reading out data from the address; and

the collecting step includes the step of adding the address under test to the set of failed address information, if the written set of data is not equivalent to the set of data read-out.

7. The method of claim 6 wherein the collecting step includes the step of:

adding bit locations in the address under test, in which the written set of data differs from the set of data read-out, to the set of failed address information.

8. The method of claim 1, further including the step of:

repairing the chip using redundancy allocation techniques based on the set of failure information.

9. The method of claim 1 further comprising the steps of:

identifying a number of circuit redundancies within the chip; and

halting testing if the failure information exceeds the number of redundancies.

10. A data structure for transmitting failed memory information from an on-chip built in self-test circuit over a communications link to a computer, comprising:

a failed address field; and

a failed bit locations field.

11. The data structure of claim 3 further comprising:

a header field;

a failed address length field;

a failed data length field;

a data written field; and

a data read-out field.

12. A method for chip testing, comprising the steps of:

establishing a communications link between a chip and a computer tester;

receiving on the chip an initial test algorithm over a communications link;

testing a memory array within the chip, using a built-in self-test circuit (BIST) on the chip, in accordance with the initial test algorithm;

adding an address under test and those bit locations which failed to a set of failed address information, if a set of data written to the address under test is not equivalent to a set of data read-out from the address under test;

transmitting the failed address information from the chip to the computer over the communications link; and

generating a bit-map on the computer, from the failed address information, of the failed bit locations within the memory array.

13. A computer-usable medium embodying computer program code for commanding a computer to perform chip testing comprising the steps of:

establishing a communications link between a chip and a computer tester;

receiving on the chip an initial test algorithm over a communications link;

testing the chip, using a built-in self-test circuit (BIST) on the chip, in accordance with the initial test algorithm;

collecting a set of failure information in response to the testing; and

transmitting the failure information from the chip to the computer over the communications link.

14. The medium of claim 13, wherein the testing step includes the step of:

testing a memory array within the chip in accordance with the algorithm.

15. The medium of claim 14 further comprising the step of:

generating a bit-map on the computer, from the failure information, of failed bit locations within the memory array.

16. The medium of claim 14 wherein the collecting step includes the step of:

collecting a set of failed address information in response to the testing.

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17. The medium of claim 16 wherein:

the testing step includes the steps of,

writing a set of data to an address under test in the memory array

reading out data from the address; and

the collecting step includes the step of adding the address under test to the set of failed address information, if the written set of data is not equivalent to the set of data read-out.

18. The medium of claim 17 wherein the collecting step includes the step of:

adding bit locations in the address under test, in which the written set of data differs from the set of data read-out, to the set of failed address information.

19. The medium of claim 13, further including the step of:

repairing the chip using redundancy allocation techniques based on the set of failure information.

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20. A system for chip testing comprising a:

means for establishing a communications link between a chip and a computer tester;

means for receiving on the chip an initial algorithm over a communications link;

means for testing the chip, using a built-in self-test circuit (BIST) on the chip, in accordance with the initial test algorithm;

means for collecting a set of failure information in response to the testing; and

means for transmitting the failure information from the chip to the computer over the communications link.

21. A system for chip testing, comprising:

a communications link;

a computer, operating a set of chip testing software; and

a chip under test coupled to the computer by the communications link, having,

a memory array; and

a Built In Self Test (BIST) module for testing the memory array in response to test algorithms received from the computer and transmitting those addresses within the memory array which failed testing.

22. The system of claim 21, wherein the chip includes:

redundant circuits responsive to repair programs activated on the computer in response to the address failures detected during testing.